Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A static random access memory (SRAM) comprising:

at least a first wire;

at least a second wire;

a plurality of word lines;

a plurality of pairs of bit lines;

a plurality of SRAM cells for storing data, each of the SRAM cells is connected to the first wire, the second wire, a corresponding word line, and a corresponding pair of the bit lines;

a first bias terminal for inputting V_{DD};

a second bias terminal for inputting V_{SS};

at least a first capacitor connected to the first wire for maintaining a voltage level of the first wire above a first predetermined voltage level;

at least a second capacitor connected to the second wire for maintaining a voltage level of the second wire below a second predetermined voltage level;

at least a first switch unit connected between the first bias terminal and the first wire having a first control terminal for inputting a first control signal, wherein the first switch unit is turned on by the first control signal during

read/write operations of the SRAM cells; and
at least a second switch unit connected between the second bias terminal and the second wire having a second control terminal for inputting a second control signal, wherein the second switch unit is turned on by the second control signal during read/write operations of the SRAM cells.

[c2] 2.The static random access memory of claim 1 wherein when the SRAM cells are not accessed, the first switch unit and the second switch unit are turned off so that two power terminals of each of the SRAM cells disconnect from V_{DD} and Vss.

3.The static random access memory of claim 1 wherein when the SRAM cells are not accessed and the voltage level of the first wire approaches the first predetermined voltage level, the first switch unit is turned on so that the first capacitor is charged via V_{DD} and that a difference between the voltage level of the first wire and the first predetermined voltage level is increased.

[c3] 4.The static random access memory of claim 1 wherein when the SRAM cells are not accessed and the voltage level of the second wire approaches the second predetermined voltage level, the second switch unit is turned on so that the second capacitor is charged via V_{SS} and that a difference between the voltage level of the second

wire and the second predetermined voltage level is increased.

[c4] 5.The static random access memory of claim 1 wherein the first control signal and the second control signal are conjugate to each other.

[c5] 6.The static random access memory of claim 1 wherein the first capacitor and the second capacitor are intrinsic capacitances of the SRAM cells.

[c6] 7.A static random access memory comprising:
a first bias terminal for inputting V_{DD};
a second bias terminal for inputting V_{SS};
a plurality of word lines;
a plurality of pairs of bit lines; and
a plurality of SRAM rows, each of the SRAM rows comprising:
a first wire;
a second wire;
a plurality of SRAM cells for storing data, each of the SRAM cells is connected to the first wire, the second wire, a corresponding word line, and a corresponding pair of the bit lines;
a first capacitor connected to the first wire for maintaining a voltage level of the first wire above a first predetermined voltage level;

a second capacitor connected to the second wire for maintaining a voltage level of the second wire below a second predetermined voltage level;

a first switch unit connected between the first bias terminal and the first wire having a first control terminal for inputting a corresponding first control signal, wherein the first switch unit is turned on by the first control signal during read/write operations of the SRAM cells; and

a second switch unit connected between the second bias terminal and the second wire having a second control terminal for inputting a corresponding second control signal, wherein the second switch unit is turned on by the second control signal during read/write operations of the SRAM cells.

[c7] 8.The static random access memory of claim 7 wherein when the SRAM cells of each SRAM row are not accessed, the first switch unit and the second switch unit of the SRAM row are turned off so that two power terminals of each of the SRAM cells of the SRAM row disconnect from V_{DD} and Vss.

9.The static random access memory of claim 7 wherein when the SRAM cells of each SRAM row are not accessed and the voltage level of the first wire of the SRAM row approaches the first predetermined voltage level, the first switch unit of the SRAM row is turned on so that the

first capacitor of the SRAM row is charged via V_{DD} and that a difference between the first predetermined voltage level and the voltage level of the first wire of the SRAM row is increased.

[c8] 10.The static random access memory of claim 7 wherein when the SRAM cells of each SRAM row are not accessed and the voltage level of the second wire of the SRAM row approaches the second predetermined voltage level, the second switch unit of the SRAM row is turned on so that the second capacitor of the SRAM row is charged via V_{SS} and that a difference between the second predetermined voltage level and the voltage level of the second wire of the SRAM row is increased.

[c9] 11.The static random access memory of claim 7 wherein the first control signals and the second control signals are conjugate to each other.

[c10] 12.The static random access memory of claim 7 wherein the first capacitors and the second capacitors are intrinsic capacitances of the SRAM cells.

[c11] 13.The static random access memory of claim 7 wherein the first switch units and the second switch units are turned on sequentially.

[c12] 14.A static random access memory comprising:

a plurality of SRAM cells for storing data;

at least a first switch unit;

at least second switch unit; and

at least capacitor;

wherein during read/write operations of the SRAM cells, the first switch unit and the second switch unit are turned on so that two power terminals of each SRAM cells are electrically connected to V_{DD} and V_{SS} respectively and that the capacitor is electrically connected between V_{DD} and V_{SS}, and when the SRAM cells are not accessed, the first switch unit and the second switch unit are turned off so that the two power terminals of each SRAM cell electrically disconnected from V_{DD} and V_{SS} and the capacitor maintains a voltage gap between the two power terminals greater than a predetermined voltage value.

[c13] 15.The static random access memory of claim 14 wherein the first switch unit is connected to V_{DD}, the first switch unit is connected to V_{SS}, one of two terminals of the capacitor is connected to the first switch unit, and the other terminal of the two terminals of the capacitor is connected to V_{SS}.

[c14] 16.The static random access memory of claim 14 wherein the first switch unit is connected to V_{DD}, the first switch unit is connected to V_{SS}, one of two terminals of

the capacitor is connected to the second switch unit, and the other terminal of the two terminals of the capacitor is connected to V_{DD}.

[c15] 17.The static random access memory of claim 1 wherein the capacitor is an intrinsic capacitance of the SRAM cells.